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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/316,560	05/24/1999	MARC DURANTON	PHF-99.540V	7958

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	38

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/316,560	DURANTON, MARC	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4-5 are objected to because of the following informalities:

As per claim 4, line 13, add --the control unit-- before "controls".

As per claim 5, lines 13-14, "the step-up signal" should be --the set-up signals--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Torii et al. (4,734,850).

As per claim 5, Torii et al. teaches a system including an E-unit 5 ("first processor") and a FIFO 21, and an E-unit 1 ("second processor"). The E-unit 1 receives input from E-unit 5 ("providing successive sets of input data...receiving successive sets of output data"). See column 2, lines 9-14. With reference to figure 2, FIFO 21 is comprised of 2 memory banks 47, 48 ("plurality of memory circuits"). The receipt of successive sets of input data that is written into the memory banks is described at column 5, line 65, to column 6, line 6, and receiving successive sets of output data that is read from the memory banks is described at column 7, lines

38-52. A mode indicating circuit 41 indicates a write mode, which selects which bank is written or read, and therefore selects how a bank is addressed (either for writing or reading). See column 3, lines 26-43, and figures 3A-B, which shows the particular modes for each memory bank.

A write counter, CNT 64 (figure 4), receives signal WREQ ("set-up signals from the first processor"), where CNT 64 indicates the write address of the bank. See column 9, line 60, to column 10, line 8. A read counter, CNT 109 (figure 5), receives signal RREQ ("set-up signals from the second processor") and indicates the read address (see column 14, lines 29-34 and 57-59). Based on the selected mode signal SW from the mode indicating circuit, and the initialization of the counters, CNT 64 and CNT 109, asynchronous writing and reading from the memory banks of a FIFO circuit is performed. See, in general, figure 6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (5,027,330) in view of Hubbins et al. (4,698,753).

As per claims 1 and 4, Miller teaches a system incorporating an asynchronous FIFO circuit. The system includes, with reference to figure 3, an input processor 5 ("first processor") for writing to the FIFO and an output processor 15 ("second processor") for reading from the

FIFO. See also column 2, lines 3-9. The memory circuit includes a plurality of FIFO circuits 100, 150. The reset circuit 215 and flag circuit 210 represent the "master controller" of claim 1. FIFO status signals and the reset signal 8 represent "control commands". The system of Mason also includes a write control circuit 205, write pointer 235, read control circuit 220, and a read pointer 245 (collectively a "control unit", where the pointers are actually counters incremented based on signals from their respective control circuits). These pointers are loaded based on a write enable signal from the input processor and read enable signals received from the output processor. See figure 2 and column 3, lines 37-66.

Miller does not teach that the write pointer register 235 and the read pointer register 245 are loaded with variable, non-zero values, i.e. a write or read start address. Hubbins et al. teaches that it was known to explicitly load by requesting processors write and/or read start addresses and thereafter use pointer auto-increment to step through successive locations in the buffer (RAM). See column 3, lines 45-50. It would have been obvious to one of ordinary skill in the art to have modified Miller such that the registers 235, 245 are loaded with the appropriate write or read start address, as taught by Hubbins et al., because Hubbins et al. teaches that this would allow designating buffer areas within the FIFO RAM (see column 3, lines 45-46), which would allow greater flexibility in the system by allowing multiple designated buffer areas in the FIFO RAM for access, thereby holding multiple, independent data streams.

As per claim 2, as set forth previously, Miller teaches a write pointer and a read pointer, which indicate the addresses to which data is written and read from.

As per claim 3, Miller teaches, with reference to figures 2-3, read port (elements 2 and "output data bus" 11) and write port (element 7 and "input data bus" 6).

As per claim 4, Miller teaches a flag circuit 210 (figure 2), which indicates when the FIFO is empty (E), half-full (HF), and full (F). See column 2, lines 55-60. This circuit tracks the difference in the values between the read and write pointers and outputs the E, HF, or F signals based on the difference. See column 1, lines 19-24. This process is performed in part so that the FIFO rejects any attempt to store data in the memory when full (i.e. preventing the read and write pointers from simultaneously trying to access the same memory location). See column 1, lines 34-44. The "comparator" is represented by the element that determines the difference between the read and write pointers.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Csoppenszky et al. (5,852,608) in view of Hubbins et al. (4,698,753).

As per claims 1 and 4, Csoppenszky et al. teaches a system for bi-directional transfers between a first system and a second system. The first and second systems can include various computer-based systems (see column 2, lines 36-37), such as two processors (wherein the two processors would have asynchronous clock signals). The system includes a dual-port memory, which would inherently have a plurality of addressable locations ("memory circuits"), where the dual-port memory is accessible by both systems for transferring data between the systems. With reference to figure 2, the direction control circuit 3 ("master controller") sets up the dual port memory system, based on signals ("master controller") from the systems, for transfer between the systems, for example from system A to system B. See column 3, line 65, to column 4, line 22.

Csoppenszky et al. also teaches a write register 209 and a read register 210, which are individually loaded from each system, both part of the control unit, comprised of elements 300

and 400. For example, when transferring data from system A to system B, WAD_A loads an address into register 209 and RAD_B loads an address into register 210. See column 6, lines 1-7 and 29-34.

Csoppenszky et al. does not teach that the registers 209 and 210 are counters. Hubbins et al. teaches explicitly loading by requesting processors write and/or read start addresses and thereafter using pointer auto-increment (i.e. a counter) to step through successive locations in the buffer (RAM). See columns 3, lines 45-50. It would have been obvious to one of ordinary skill in the art to have modified Csoppenszky et al. to utilized pointer auto-increment after loading the start write and/or read addresses into the appropriate registers, as taught by Hubbins et al., because Hubbins et al. teaches that such an arrangement would permit buffer management functions to be performed in hardware by the device with little software overhead (see column 3, lines 50-53).

As per claim 2, the combination of Csoppenszky et al. and Hubbins et al. teaches write and read counters as detailed above for claim 1.

As per claim 3, Csoppenszky et al. teaches a write enable system A signal, WEN_A, and a read enable system B signal, REN_B, both input into the control circuit.

As per claim 4, with respect to the comparator, Csoppenszky et al. teaches determining when the memory is empty or full, in order to prevent read or write operations to the same memory location (see column 7, lines 43-50). It is inherent that a comparator is utilized to determine whether the read address value equals (or almost equals) the write address value.

Response to Arguments

7. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendments to the claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wyland (5,261,064) teaches burst memory including counter loaded with burst start access addresses.

Liu et al. (5,696,940) teaches a FIFO RAM that includes loading counters with read and write start addresses.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
June 14, 2004